ABSTRACT AMENDMENTS

Replace the Abstract with:

A semiconductor device TSOP (Thin Small Outline) Package includes upper and lower semiconductor chips arranged between a first lead portion and a second lead portion, respectively, on two opposing sides of the semiconductor device, in plan view. A first die pad is integrated with and not coplanar with the first lead portion and is located on one side of a reference plane passing through a central position between a first surface and a second surface of the first and second lead portions. A second die pad is integrated with and not coplanar with the second lead portion and is located on a second side of the reference plane. The lower semiconductor chip is supported by the first die pad and the upper semiconductor chip is supported by the second die pad portion. The upper and lower semiconductor chips are partially overlapping and overlap in height with the first and second lead portions.